REMARKS

The present application was filed on December 18, 2001 with claims 1 through 22. Claims 3-6, 11, 13 and 14 were previously cancelled herein, without prejudice, and claims 23 through 29 were previously added. Claims 1, 2, 7-10, 12 and 15-29 are presently pending in the above-identified patent application. Claim 12 and 16 are proposed to be amended herein.

In the Office Action, the Examiner rejected claim 12 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Claims 16-22 were rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. The Examiner rejected claims 16-19 and 22 under 35 U.S.C. §102(e) as being anticipated by Raghavan (United States Patent No. 6,418,172). In addition, the Examiner rejected claims 1, 2, 8, 9, 15, 23, 24 and 26-29 under 35 U.S.C. §103(a) as being unpatentable over Spinnler ("Design of Hyper States for Reduced – State Sequence Estimation") in view of Raghavan. The Examiner rejected claims 120 and 21 under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Spinnler. Claims 10, 12 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Spinnler and Raghavan and further in view of Polydoros (United States Patent No. 5,432,821).

Section 112 Rejection

Claim 12 was rejected under 35 U.S.C. §112, second paragraph, because it depended from a cancelled claim. Claim 12 has been amended to correct the error.

Section 101 Rejection

Claims 16-22 were rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. The Examiner asserts that claim 16 is directed solely to an abstract idea.

The Supreme Court has stated that the "[t]ransformation and reduction of an article 'to a different state or thing' is the clue to patentability of a process claim." *Gottshalk v. Benson*, 409 U.S. 63, 70, 175 U.S.P.Q. (BNA) 676 (1972). In other words, claims that require some kind of transformation of subject matter, which has been held to include intangible subject matter, such as data or signals, that are representative of or constitute physical activity or objects have been held to comply with Section 101. *See, for example, In re Warmerdam,* 31 U.S.P.Q.2d

(BNA) 1754, 1759 n.5 (Fed. Cir. 1994) or *In re Schrader*, 22 F.3d 290, 295, 30 U.S.P.Q.2d (BNA) 1455, 1459 n.12 (Fed. Cir. 1994).

Thus, as expressly set forth in claim 16, the claimed method represents an MLT-3 code as a trellis, where the MLT-3 code uses three *signal levels* (physical things) to represent two binary values. The claimed method generates a trellis with a plurality of trellis states, each of the trellis states associated with a *value for a signal* in a previous symbol period. In addition, each of the trellis states has at least two branches leaving or entering each state, with each of the at least two branches corresponding to state transitions associated with the two binary values. A first binary value *causes* a state transition in the trellis and a second binary value does not cause a state transition in said trellis.

This transformation to a trellis representation of an MLT-3 code provides a useful, concrete and tangible result.

Applicant submits that claim 16 is in full compliance with 35 U.S.C. §101, and accordingly, respectfully requests that the rejection under 35 U.S.C. §101 be withdrawn.

Prior Art Rejections

Claim 16-19

Claims 16-19 and 22 were rejected under 35 U.S.C. §102(e) as being anticipated by Raghavan. The Examiner asserts that Raghavan discloses a method for representing an MLT-3 code as a trellis, said MLT-3 code using three signal levels to represent two binary values, the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period; and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values. (citing FIG. 1A and col. 3, lines 37-50).

Raghavan, however, discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A). Independent claim 16 has been amended to emphasize that the first binary value substantially always causes a state transition in the trellis from a first state to a *different* state. Support for this amendment can be found in the original specification, for example, at in Figure 5, and page 4,

lines 17-18. It is noted that the term "substantially" is a proper broadening modifier to avoid reliance on the doctrine of equivalents in an infringement actions. See In re Wiggins, 488 F. 2d 538, 541, 179 USPQ 421, 423 (CCPA 1973).

In Raghavan, however, Fig.1A shows that the input value 1 *sometimes* causes a transition into the same state, and sometimes a transition into a different state.

Thus, Raghaven does not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value *substantially always* causes a state transition in said trellis *from a first state to a different state* and a second binary value does not cause a state transition in said trellis," as required by claim 16, as amended.

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Spinnler in view of Raghavan.

Regarding claims 1 and 8, the Examiner asserts that Spinnler discloses decoding an encoded signal received from a dispersive channel causing intersymbol interference by generating at least one trellis representing the code and the channel and peforming joint equalization and decoding of the received signal using the trellis (citing, Abstract and Section 1, Page 1).

The Examiner acknowledges that Spinnler does not disclose that the signal is encoded using the MLT-3 code, but cites Raghavan for this purpose.

In order to establish a *prima facie* case of obviousness, the following three criteria must be met:

> [f]irst, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

M.P.E.P. §2143. Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references.

First, MLT-3 codes are not trellis coded modulation (TCM) as described by Spinnler. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention.

In addition, as discussed hereinafter, if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense, that is the number of states would be *fractional*. Thus, a person of ordinary skill in the art would not make such a combination.

In particular, the number of states in Spinnler is given by equation (2) in Spinnler. For MLT-3, Zs=4 and Ma=3 (the size of channel symbol alphabet in MLT-3 equals 3, as the channel symbols are -1,0,1). Therefore, Spinnler's equation yields $4x(3/2)^{(L-1)}$.

The trellis of the present invention, on the other hand, has a number of states given by $4x(2^K)$, where K is the truncated channel memory.

It is further noted that Spinnler's equation uses the channel memory (L-1), while the present invention use the truncated memory K. See, for example, page 6, lines 15-16.

In addition to providing a fractional number of states, which suggests away from the combination, the number of states associated with the present invention ($4x(2^K)$,) is lower than Spinnler ($4x(3/2)^{(L-1)}$). This is a "surprising result" which is further evidence of non-obviousness.

Dependent Claims

Dependent claims 2, 7, 9-10, 12, 15 and 17-29 were rejected under 35 U.S.C. §§102(e) or 103(a) as being anticipated by or unpatentable over Raghavan, Spinnler and Polydoros, alone or in combination.

Claims 2, 7, 9-10, 12, 15 and 17-29 are dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Spinnler and Polydoros (alone or in any

combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

With regard to Claim 10, for example, the Examiner acknowledges that Spinnler and Raghaven do not disclose a BMU that calculates branch metrics based on the received signal and an ACSU that determines the best surviving path into the reduced states; and a DFU that takes survivor symbols from the SMU to calculate ISI estimates for the reduced states, wherein the ISI estimates are used by the BMU to calculate branch metrics for transitions in the reduced-state trellis. The Examiner asserts that these limitations are shown by Polydoros.

The Examiner asserts the channel estimator 102 of FIG. 13 is a DFU that takes survivor symbols from the SMU to calculate ISI estimates for the reduced stateswherein the ISI estimates are used by the BMU to calculate branch metrics for transitions in the reduced-state trellis. Block 102 of Polydoros, however, is a channel estimator. A channel estimator estimates *channel coefficients,* f_k. The DFU required by claim 10, however, does not estimate channel coefficients, f_k, but rather claim 10 requires that the DFU computes *ISI estimates.*

As described on page 7 of the present specification, the decision-feedback unit (DFU) takes the survivor symbols from the SMU to calculate the ISI estimates for the reduced states, which are used by the BMU to calculate the branch metrics for the transitions in the reduced-state trellis. The receiver 900 can be embodied in a similar manner to the 1000BASE-T RSSE decoder described in E.F. Haratsch and K. Azadet, "A 1-Gb/s Joint Equalizer and Trellis Decoder for 1000BASE-T Gigabit Ethernet," IEEE J. Solid-State Circuits, vol. 36, 374-384 (Mar. 2001) or United States Patent Application Serial Number 09/471,920, filed Dec. 23, 1999, entitled "Method and Apparatus for Shortening the Critical Path of Reduced Complexity Sequence Estimation Techniques," each incorporated by reference herein.

An ISI estimate is defined as sum of products of channel coefficients and survivor symbols as shown in Fig. 8 of E.F. Haratsch and K. Azadet, "A 1-Gb/s Joint Equalizer and Trellis Decoder for 1000BASE-T Gigabit Ethernet," IEEE J. Solid-State Circuits, vol. 36, 374-384 (Mar. 2001).

With regard to claim 25, Applicants query where, in particular, Polydoros discloses that ISI estimates are being computed.

With regards to claims 26 and 29, Applicants refer the Examiner to the above discussion regarding the number of states.

Conclusion

All of the pending claims, i.e., claims 1, 2, 7-10, 12 and 15-29, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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